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Project 4 Report

**Description**: This project was about creating four 1-bit adders, which equaled to one 4-bit adder and then creating a 16-bit adder, by creating four 4-bit adders. This project was significant because it showed in depth, how an adder functions specifically through the Verilog. Also, I learned how to make the 16-bit adder, to add the values when a input is equal to 0 and subtract the values when a input is equal to 1.

**Discussion**: The difference between the first simulation and the second simulation is that the first simulation showed the function of the adder with instant results, while the second simulation showed delays. This is important because the first simulation allowed me to understand what was happening in the adder, while the second simulation allowed me to witness actual delays that occur in real life, which many people choose to ignore or forget about.

**What I Have Done:** I copied the Verilog for the four 1-bit adder from the pdf file provided on Beachboard. I then copied down the test bench, which allowed me to simulate the function. I then made changes to the Verilog code by adding “#5” and “#7”, which added a delay in the simulation, showing how the adder would function in real life. I wrote these changes down and moved on to creating another function called “mux,” which had a input titled “add\_sub” which either added the inputs or subtracted the inputs depending on whether if it was on or off.